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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,944	10/10/2003	Steven P. Young	X-1392-1P US	2771

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,944	YOUNG, STEVEN P.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *17-23 and 30-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-16,24-26,28 and 29* is/are rejected.

7)☒ Claim(s) *12 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-10-03,10-16-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-16 and 24-29, drawn to an integrated circuit having circuitry arranged in an array having columns and rows, classified in class 326, subclass 38.

II. Claims 17-23 and 30-33, drawn to a method of generating a circuit layout, classified in class 716, subclass 9.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and Group II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions are a structure of an integrated circuit arranged in an array format classified in class 326/36 while Group II pertains to a method of generating a circuit layout classified in class 716/9.Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Kim Kanzaki on March 17, 2005 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-16 and 24-29. Affirmation of this election must be made by applicant in replying to this Office action. Claims 17-23 and 30-33 are withdrawn from further

consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11, 13-16, 24-26 and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Langhammer et al. (US PAT No. 6,538,470).

Regarding claim 1, Figs. 5 and 9 of Langhammer et al. teaches an integrated circuit (IC), including circuitry arranged in an array having a plurality of rows and a plurality of columns (Fig. 5 shows columns and rows), where each row of the plurality of rows begins at a first side of the IC and ends at a second side of the IC (from left to right of 106), and each column of the plurality of columns begins at a third side of the IC and ends at a fourth side of the IC (top to bottom of 106), the IC comprising: a column of the plurality of columns comprising a plurality of circuit elements of a circuit type substantially occupying the column (Fig. 9 is a floor plan of Fig. 5 where each column is filled with LAB, I/O INPUT REG...); and a row of the plurality of rows positioned at the third side of the IC, where a number of circuit elements of, an input and output circuit type in the row is less than a number of remaining circuit elements of other circuit types in the row (each row has two I/O blocks, 128 which is less than remaining types).

Regarding claim 2, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 1 where the circuit type is selected from a group (group consisting of LAB, I/O, REG, MULTIP, ADD/SUB) consisting of a Configurable Logic Block type, a Multi-Giga Bit Transceiver type, a Block Random Access Memory type, a Digital Signal Processor circuit type, a multiplier circuit type, an arithmetic circuit type (ADD/SUB), an Input/output Interconnect circuit type, an Input/output Block type, and an application specific circuit type.

Regarding claim 3, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 1 where the input and output circuit type is an Input/output Block (IOB) type (I/O).

Regarding claim 4, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 1 where the input and output circuit type includes an Input/output Block type and a Multi-Giga Bit Transceiver type (128 provides interface for digital signal processing block with more than one bit data, i.e. multi-giga bits, e.g. 18 bits of data and 2 bits of control information; col. 15, lines 45-62).

Regarding claim 5, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 1 further comprising a center column comprising configuration logic (PIPELLINE w/BYPASS, 138, is a logic circuit configured to selectively bypass the registering of the digital processing signals; col. 18, lines 40-60).

Regarding claim 6, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 3 where the center column is positioned on or near the center of axis of the IC (138 is on center).

Regarding claim 7, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 4 further comprising a clock column adjacent to the center column (Fig. 10 shows column 110, which provides two sets of clock and clear signals,158).

Regarding claim 8, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 1 where the column of the plurality of columns further comprises a spacer tile (Fig. 10 shows a space between each column) and a clock tile (tile 110 having a clock signals).

Regarding claim 9, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 1 further comprising an embedded processor (110 is a digital signal processor).

Regarding claim 10, Figs. 5 and 9 of Langhammer et al. teaches an integrated circuit, comprising circuitry having programmable functions (LABs) and programmable interconnects (interconnect structure shown in Figs. 3 and 4), the IC further comprising: a plurality of homogeneous columns (LAB columns, I/O columns, input reg columns...) and wherein each of the homogeneous columns starts at one side of the IC and ends at

an opposite side of the IC (starts at the top and end at the bottom of the floor plan), and wherein a first column of the plurality of homogeneous columns comprises a first set of substantially identical circuit elements of a first circuit type (LABs) substantially filling the first column.

Regarding claim 11, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 10: wherein a second column of the plurality of homogeneous columns comprises a second set of substantially identical circuit elements of a second circuit type (I/O) substantially filling the second column, and wherein a third column of the plurality of homogeneous columns comprises a third set of substantially identical circuit (INPUT REG) elements of a third circuit type substantially filling the third column.

Regarding claim 13, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 10 where the first circuit type is selected (LAB is selected for the first column from a group consisting of LAB, I/O, REG, MULTIP, ADD/SUB) from a group consisting of a Configurable Logic Block, a Multi-Giga Bit Transceiver (MGT) type, a Block Random Access Memory, a fixed logic type, an Input/Output Interconnect , and an Input/Output Block type .

Regarding claim 14, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 13 where the fixed logic type comprises a Digital Signal Processor (110 is a digital signal processor having MULTIP, ADD/SUB, OUTPUT SEL/REG, PIPELINE

w/ BYPASS), a multiplier circuit type, an arithmetic circuit type, an application specific circuit type.

Regarding claim 15, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 10 where the integrated circuit further comprises a field programmable gate array (FPGA is a programmable logic device).

Regarding claim 16, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 10 where integrated circuit further comprises a programmable logic device (see ABSTRACT).

Regarding claim 24, Figs. 5 and 9 of Langhammer et al. teaches an integrated circuit comprising: a plurality of columns (see Fig. 9) and wherein each of the columns starts at one side of the IC and ends at an opposite side of the IC (top side to bottom side of Fig. 9), wherein a first column of the plurality of columns comprises a first set of substantially identical circuit elements of a first circuit type (LAB filled in the first column) substantially filling the first column, wherein a second column of the plurality of columns comprises a second set of substantially identical circuit elements of a second circuit type (I/O filled in the second column) substantially filling the second column, and wherein a third column of the plurality of columns comprises a third set of substantially identical circuit elements of a third circuit type (INPUT REG) substantially filling the third column.

Regarding claim 25, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 24 further comprising circuitry having programmable functions and programmable interconnects (LABs are programmable and the interconnection shown in Figs. 3 and 4).

Regarding claim 26, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 25 where the first, second, and third circuit types have a circuit type selected (the selected first, second and third types are LAB, I/O, and INPUT REG respectively) from a group (group consisting of LAB, I/O, REG, MULTIP, ADD/SUB) consisting of a Configurable Logic Block (LAB) type, a Multi-Giga Bit Transceiver type, a Block Random Access Memory type, a Digital Signal Processor, an arithmetic circuit type , an Input/output Interconnect circuit type, an Input/output Block type, and an application specific circuit type.

Regarding claim 28, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 24 where the substantially identical circuit elements are substantially identical tiles (LABs are substantially identical tiles).

Regarding claim 29, Figs. 5 and 9 of Langhammer et al. teaches the integrated circuit of claim 28 wherein each tile comprises a functional element coupled to a switch matrix (Fig. 3 and 4 shows interconnect matrix).

Allowable Subject Matter

Claims 12 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Langhammer et al. teaches the programmable logic integrated circuit device with programmable logic and a dedicated digital signal processing region, one of ordinary skill in the art would not have been motivated to modify the teaching of Langhammer et al. to further includes, among other things, the specific of a heterogeneous center column having configurable logic, a clock management circuit element, and an input/output block as required by claims 12 and 27.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Seefeldt et al. (US PAT No. 4,978,633) discloses a variable die size array architecture.

Bilski et al. (US PAT No. 6,803,786) discloses structures and methods of including processor capabilities in an existing PLD architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

Date: 3-17-2005